

Amendments to the Claims

The listing of claims below will replace all prior versions and listings of claims in the present application.

Claim Listing

1 1. (Currently Amended) An apparatus for switching packets, each packet having
2 a header portion, ~~an optional~~ a corresponding tail portion, and a class of service indicator,
3 said apparatus comprising:

4 a pipelined switch comprising:

5 a plurality of packet header buffers (PHBs);

6 an equal plurality of PHB pointers, each said PHB pointer pointing to a
7 corresponding PHB; and

8 an equal plurality of pipeline stage circuits connected in a sequence,
9 comprising at least a first stage circuit and a last stage circuit,

10 wherein:

11 each said stage circuit begins an operation substantially
12 simultaneously with each other;

13 each said stage circuit passes data to a next stage circuit in said
14 sequence when every said operation performed by all said
15 stage circuits is completed;

16 said first stage circuit reads said header portion and stores said
17 header portion in said corresponding PHB using said
18 corresponding PHB pointer; and

19 said last stage circuit outputs a modified header portion; and

20 a receive buffer manager (RBM) comprising:

21 a joining circuit connected to said pipelined switch wherein said modified
22 header portion and said corresponding tail portion are joined to
23 form a modified packet;

24 a receive queue manager connected to said joining circuit that buffers said
25 modified packet in a receive packet buffer and enqueues said

26 modified packet using said class of service indicator and a plurality
 27 of receive queues; and
 28 a dequeue circuit connected to said receive queue manager and said
 29 receive packet buffer, wherein said dequeue circuit uses said class
 30 of service indicator to dequeue said modified packet to a switch
 31 fabric.

1 2. (Original) The apparatus as recited in Claim 1, wherein said plurality of
 2 pipeline stage circuits further comprise:
 3 a pre-process circuit connected to said first stage circuit, wherein said pre-process
 4 circuit uses a second said PHB pointer to record first data in said
 5 corresponding PHB;
 6 a pointer lookup circuit connected to said pre-process circuit that compares said
 7 header portion to a first data structure and determines a leaf pointer using
 8 said second PHB pointer;
 9 a table lookup circuit connected to said pointer lookup circuit that uses said leaf
 10 pointer to access one or more sets of linked data structures and to fetch
 11 second data, wherein said table lookup circuit uses a third said PHB
 12 pointer to record said second data in said corresponding PHB; and
 13 a post-process circuit using said third PHB pointer and connected to said table
 14 lookup circuit, wherein said post-process circuit uses a fourth said PHB
 15 pointer to record third data in said corresponding PHB;
 16 wherein said last pipeline stage circuit comprises a gather circuit connected to said post-
 17 process circuit, and wherein said gather circuit uses said fourth PHB pointer to assemble
 18 said modified header portion.

1 3. (Original) The apparatus as recited in Claim 1, further comprising:
 2 an input device that receives said packet; and
 3 a first buffer connected between said input device and said first stage circuit,
 4 wherein said first buffer buffers said header portion and said tail portion.

1 4. (Original) The apparatus as recited in Claim 3, further comprising a
2 multiplexer interposed between said first buffer and said first stage circuit, wherein said
3 multiplexer multiplexes said header portion and said corresponding tail portion together.

4 5. (Original) The apparatus as recited in Claim 1, further comprising a second
5 buffer interposed between said last stage circuit and said joining circuit.

1 6. (Original) The apparatus as recited in Claim 5, further comprising a
2 multiplexer interposed between said last stage circuit and said second buffer, wherein
3 said multiplexer multiplexes said modified header portion and said corresponding tail
4 portion together.

1 7. (Original) The apparatus as recited in Claim 1, wherein said receive packet
2 buffer comprises buffers of different sizes.

1 8. (Original) The apparatus as recited in Claim 1, wherein said receive packet
2 buffer comprises buffers of equal size.

1 9. (Original) The apparatus as recited in Claim 1, wherein said receive queue
2 manager comprises a congestion avoidance circuit utilizing a status of each said receive
3 queue.

1 10. (Original) The apparatus as recited in Claim 9, wherein said status comprises
2 a measure of average queue depth.

1 11. (Original) The apparatus as recited in Claim 1, further comprising a transmit
2 buffer manager (TBM), said TBM comprising:
3 a third buffer that receives one or more packets from said switch fabric;
4 a transmit queue manager connected to said third buffer that buffers each said
5 packet in a transmit packet buffer and enqueues said packet using said
6 class of service indicator and a plurality of transmit queues; and

7 a dequeue circuit connected to said transmit queue manager and said transmit
 8 packet buffer, wherein said dequeue circuit uses said class of service
 9 indicator to dequeue each said packet.

1 12. (Original) The apparatus as recited in Claim 11, wherein said transmit packet
 2 buffer comprises buffers of different sizes.

1 13. (Original) The apparatus as recited in Claim 11, wherein said transmit packet
 2 buffer comprises buffers of equal size.

1 14. (Original) The apparatus as recited in Claim 11, wherein said transmit queue
 2 manager comprises a congestion avoidance circuit utilizing a status of each said transmit
 3 queue.

1 15. (Original) The apparatus as recited in Claim 14, wherein said status
 2 comprises a measure of average queue depth.

1 16. (Original) The apparatus as recited in Claim 11, further comprising a
 2 transmit FIFO connected to an output of said dequeue circuit.

1 17-22. (Cancelled)

1 23. (Currently Amended) A method of switching packets, which comprises:
 2 receiving a packet, said packet having a header portion, ~~an optional a~~
 3 corresponding tail portion, and a class of service indicator;
 4 switching said packet through a pipelined switch having a plurality of packet
 5 header buffers (PHBs), an equal plurality of PHB pointers wherein each
 6 said PHB pointer points to a corresponding PHB, and an equal plurality of
 7 pipeline stages connected in a sequence, comprising at least a first stage
 8 and a last stage, said switching further comprising:
 9 beginning said ~~sequence~~ an operation in each said stage substantially
 10 simultaneously with each other said stage;

11 passing data to a next stage circuit in said sequence when every said
 12 operation performed by all said stage circuits is completed;
 13 reading and storing said header in said corresponding PHB using said
 14 corresponding PHB pointer; and
 15 outputting a modified header portion; and
 16 buffering said modified header portion in a receive buffer manager (RBM), said
 17 buffering further comprising:
 18 joining said modified header portion and said corresponding tail portion to
 19 form a modified packet;
 20 buffering and enqueueing said modified packet using said class of service
 21 indicator; and
 22 dequeuing said modified packet using said class of service indicator.

1 24. (Original) The method of Claim 23, wherein said switching further
 2 comprises:
 3 recording first data in said corresponding PHB using a second said PHB pointer;
 4 comparing said header portion to a first data structure and determining a leaf
 5 pointer using said second PHB pointer;
 6 fetching second data using said leaf pointer to access one or more sets of linked
 7 data structures and recording said second data in said corresponding PHB
 8 using a third said PHB pointer;
 9 post-processing said header portion using said third PHB pointer and recording
 10 third data in said corresponding PHB using a fourth said PHB pointer; and
 11 assembling said modified header portion using said fourth PHB pointer.

1 25. (Original) The method of Claim 23, wherein said switching further
 2 comprises buffering said header portion and said tail portion prior to said switching.

1 26. (Currently Amended) The method of Claim 25, wherein said switching
 2 further comprises multiplexing said header portion and said tail portion together prior to
 3 beginning said sequence operation.

1 27. (Original) The method of Claim 23, wherein said buffering further comprises
2 buffering said header portion and said tail portion prior to said joining.

1 28. (Original) The method of Claim 27, wherein said buffering further comprises
2 multiplexing said header portion and said tail portion together prior to said joining.

1 29. (Original) The method of Claim 23, further comprising:
2 receiving one or more packets;
3 buffering and enqueueing each said packet using said class of service indicator and
4 a plurality of queues; and
5 dequeuing each said packet using said class of service indicator.

1 30. (Original) The method of Claim 29, wherein said buffering uses a packet
2 buffer comprising buffers of different sizes.

1 31. (Original) The method of Claim 29, wherein said buffering uses a packet
2 buffer comprising buffers of equal size.

1 32. (Original) The method of Claim 29, wherein said buffering further comprises
2 avoiding congestion using a status of each said queue.

1 33. (Original) The method of Claim 32, wherein said status comprises a measure
2 of average queue depth.

1 34. (Original) The method of Claim 29, wherein said dequeuing uses a transmit
2 FIFO.

1 35-40. (Cancelled)

1 41. (Currently Amended) A computer system for interfacing with a
 2 communications network, comprising computer instructions for:
 3 receiving a packet, said packet having a header portion, ~~an optional a~~
 4 corresponding tail portion, and a class of service indicator;
 5 switching said packet through a pipelined switch having a plurality of packet
 6 header buffers (PHBs), an equal plurality of PHB pointers wherein each
 7 said PHB pointer points to a corresponding PHB, and an equal plurality of
 8 pipeline stages connected in a sequence, comprising at least a first stage
 9 and a last stage, said switching further comprising:
 10 beginning ~~said sequence~~ an operation in each said stage substantially
 11 simultaneously with each other said stage;
 12 passing data to a next stage circuit in said sequence when every said
 13 operation performed by all said stage circuits is completed;
 14 reading and storing said header in said corresponding PHB using said
 15 corresponding PHB pointer; and
 16 outputting a modified header portion; and
 17 buffering said modified header portion in a receive buffer manager (RBM), said
 18 buffering further comprising:
 19 joining said modified header portion and said corresponding tail portion to
 20 form a modified packet;
 21 buffering and enqueueing said modified packet using said class of service
 22 indicator; and
 23 dequeuing said modified packet using said class of service indicator.

1 42. (Original) The computer system of Claim 41, wherein said switching further
 2 comprises:
 3 recording first data in said corresponding PHB using a second said PHB pointer;
 4 comparing said header portion to a first data structure and determining a leaf
 5 pointer using said second PHB pointer;

6 fetching second data using said leaf pointer to access one or more sets of linked
 7 data structures and recording said second data in said corresponding PHB
 8 using a third said PHB pointer;
 9 post-processing said header portion using said third PHB pointer and recording
 10 third data in said corresponding PHB using a fourth said PHB pointer; and
 11 assembling said modified header portion using said fourth PHB pointer.

1 43. (Original) The computer system of Claim 41, further comprising:
 2 receiving one or more packets;
 3 buffering and enqueueing each said packet using said class of service indicator and
 4 a plurality of queues; and
 5 dequeuing each said packet using said class of service indicator.

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 1 44. (Currently Amended) A computer readable storage medium, comprising
 2 computer instructions for:
 3 receiving a packet, said packet having a header portion, ~~an optional a~~
 4 corresponding tail portion, and a class of service indicator;
 5 switching said packet through a pipelined switch having a plurality of packet
 6 header buffers (PHBs), an equal plurality of PHB pointers wherein each
 7 said PHB pointer points to a corresponding PHB, and an equal plurality of
 8 pipeline stages connected in a sequence, comprising at least a first stage
 9 and a last stage, said switching further comprising:
 10 beginning ~~said sequence~~ an operation in each said stage substantially
 11 simultaneously with each other said stage;
 12 passing data to a next stage circuit in said sequence when every said
 13 operation performed by all said stage circuits is completed;
 14 reading and storing said header in said corresponding PHB using said
 15 corresponding PHB pointer; and
 16 outputting a modified header portion; and
 17 buffering said modified header portion in a receive buffer manager (RBM), said
 18 buffering further comprising:

19 joining said modified header portion and said corresponding tail portion to
 20 form a modified packet;
 21 buffering and enqueueing said modified packet using said class of service
 22 indicator; and
 23 dequeuing said modified packet using said class of service indicator.

1 45. (Original) The computer readable storage medium of Claim 44, wherein said
 2 switching further comprises:
 3 recording first data in said corresponding PHB using a second said PHB pointer;
 4 comparing said header portion to a first data structure and determining a leaf
 5 pointer using said second PHB pointer;
 6 fetching second data using said leaf pointer to access one or more sets of linked
 7 data structures and recording said second data in said corresponding PHB
 8 using a third said PHB pointer;
 9 post-processing said header portion using said third PHB pointer and recording
 10 third data in said corresponding PHB using a fourth said PHB pointer; and
 11 assembling said modified header portion using said fourth PHB pointer.

1 46. (Original) The computer readable storage medium of Claim 44, further
 2 comprising:
 3 receiving one or more packets;
 4 buffering and enqueueing each said packet using said class of service indicator and
 5 a plurality of queues; and
 6 dequeuing each said packet using said class of service indicator.

1 47. (Currently Amended) A computer data signal embodied in a carrier wave,
 2 comprising computer instructions for:
 3 receiving a packet, said packet having a header portion, ~~an optional a~~
 4 corresponding tail portion, and a class of service indicator;
 5 switching said packet through a pipelined switch having a plurality of packet
 6 header buffers (PHBs), an equal plurality of PHB pointers wherein each
 7 said PHB pointer points to a corresponding PHB, and an equal plurality of

8 pipeline stages connected in a sequence, comprising at least a first stage
9 and a last stage, said switching further comprising:
10 ~~beginning said sequence~~ an operation in each said stage substantially
11 simultaneously with each other said stage;
12 passing data to a next stage circuit in said sequence when every said
13 operation performed by all said stage circuits is completed;
14 reading and storing said header in said corresponding PHB using said
15 corresponding PHB pointer; and
16 outputting a modified header portion; and
17 buffering said modified header portion in a receive buffer manager (RBM), said
18 buffering further comprising:
19 joining said modified header portion and said corresponding tail portion to
20 form a modified packet;
21 buffering and enqueueing said modified packet using said class of service
22 indicator; and
23 dequeuing said modified packet using said class of service indicator.

1 48. (Original) The computer data signal of Claim 47, wherein said switching
2 further comprises:
3 recording first data in said corresponding PHB using a second said PHB pointer;
4 comparing said header portion to a first data structure and determining a leaf
5 pointer using said second PHB pointer;
6 fetching second data using said leaf pointer to access one or more sets of linked
7 data structures and recording said second data in said corresponding PHB
8 using a third said PHB pointer;
9 post-processing said header portion using said third PHB pointer and recording
10 third data in said corresponding PHB using a fourth said PHB pointer; and
11 assembling said modified header portion using said fourth PHB pointer.

1 49. (Original) The computer data signal of Claim 47, further comprising:
2 receiving one or more packets;

3 buffering and enqueueing each said packet using said class of service indicator and
4 a plurality of queues; and
5 dequeuing each said packet using said class of service indicator.

1 50. (Cancelled)